Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 25 (currently amended): A system comprising:

a memory array; and

a memory array controller comprising

a negative charge pump; ~~and~~

a block controller coupled to the negative charge pump, comprising:

a negative level shifter to switch an output between a read-mode voltage and an erase-mode voltage dependent upon a selection signal input;

a positive voltage switch coupled to the negative level shifter;

a bit line driver coupled to the positive voltage switch and coupled to said memory array; and

a word line driver coupled to said positive voltage switch, coupled to the negative level shifter, and coupled to said memory array; and

a second block controller to apply a signal to a second block within said memory array to read a memory cell of the second block substantially simultaneously with erasure of a first block within said memory array.

Claim 26 (original): The system of claim 25, wherein the negative level shifter comprises an output stage comprising an n-channel transistor.

Claim 27 (original): The system of claim 25, wherein the negative level shifter comprises an active pull-up circuit coupled to a current source pull-down circuit.

Claim 28 (original): The system of claim 25, wherein the erase-mode voltage comprises a high magnitude negative voltage.

Claim 29 (original): The system of claim 25, wherein the read-mode voltage comprises a low voltage current from the negative charge pump via a low resistance n-channel transistor.

Claim 30 (original): The system of claim 25, wherein said memory array comprises a block coupled to the block controller and having a bit line, a word line, and a source line.

Claim 31 (original): The system of claim 25, wherein said memory array controller comprises a block controller to apply a signal to a first block with said memory array to erase the first block.

Claim 32 (cancelled)

Claim 33 (original): The system of claim 25, wherein the negative charge pump comprises an output circuit to output the erase-mode voltage.

Claim 34 (original): The system of claim 25, wherein the negative level shifter comprises an output stage circuit coupled to said memory array to apply the erase-mode voltage to a source line of said memory array.

Claim 35 (original): The system of claim 34, wherein the output stage circuit comprises a transistor to couple the output of the negative charge pump to the source line.

Claim 36 (original): The system of claim 25, wherein the negative level shifter comprises a first circuit to pull up an output of the negative charge pump to apply a read-mode voltage to a first memory cell of said memory array.

Claim 37 (original): The system of claim 36, further comprising a second negative level shifter coupled to the negative charge pump to couple the output of the negative charge

pump to a second memory cell of said memory array substantially simultaneously with the application of the read-mode voltage to the first memory cell of said memory array.

Claim 38 (original): The system of claim 36, wherein the first circuit comprises circuitry to substantially prevent current burn within the negative level shifter.

Claim 39 (original): The system of claim 36, wherein the first circuit comprises an output stage circuit to apply a low resistance current to the first memory cell.

Claims 40-51 (cancelled)